



### **PATENT APPLICATION**

# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Attn: OIPE

Eiichi TAKAHASHI et al.

Group Art Unit: 2816

Application No.:

10/520,429

Docket No.: 1

122358

Filed: July 13, 2005

For:

DIGITAL CIRCUIT HAVING DELAY CIRCUIT FOR ADJUSTMENT OF CLOCK

SIGNAL TIMING

## REQUEST FOR CORRECTION OF PALM RECORDS

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

Attached is a photocopy of the corrected filing receipt on which errors have been corrected in red. These errors are being brought to the attention of the Patent and Trademark Office so that it may correct its records.

Respectfully submitted

James A. Oliff

Registration No. 27,075

Mario A. Costantino Registration No. 33,565

JAO:MAC/jeh

Date: October 19, 2006

OLIFF & BERRIDGE, PLC P.O. Box 19928 Alexandria, Virginia 22320 Telephone: (703) 836-6400 DEPOSIT ACCOUNT USE AUTHORIZATION Please grant any extension necessary for entry; Charge any fee due to our Deposit Account No. 15-0461



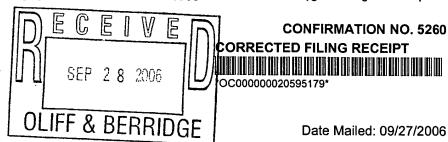
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UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

FILING OR 371 APPL NO. **ART UNIT** FIL FEE REC'D ATTY.DOCKET NO **DRAWINGS** TOT CLMS IND CLMS (c) DATE 515 10/520,429 07/13/2005 2816 122358 19 9

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### Applicant(s)

Eiichi Takahashi, Tsukuba City, JAPAN; Yuji Kasai, Tsukuba City, JAPAN; Tetsuya Higuchi, Tsukuba City, JAPAN;

### **Assignment For Published Patent Application**

National Institute of Advanced Industrial Science and Technology, Tokyo, JAPAN

Power of Attorney: The patent practitioners associated with Customer Number 25944.

### Domestic Priority data as claimed by applicant

This application is a 371 of PCT/JP03/08648 07/08/2003

### Foreign Applications

JAPAN 2002-200467 07/09/2002

If Required, Foreign Filing License Granted: 07/24/2006

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is US10/520,429

**Projected Publication Date: Not Applicable** 

Non-Publication Request: No

Early Publication Request: No

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\*\* SMALL ENTITY \*\*

Title

Digital circuit having a delay circuit for adjustment of clock signal timing

OCT 1 9 2006

Preliminary Class Digital Circuit having delay circuit for adjustment of clock signal timing

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